digital

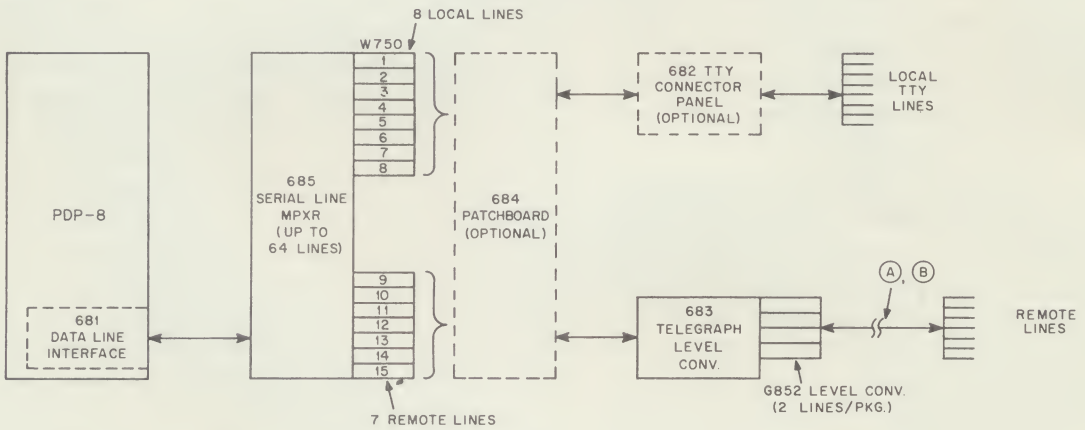
DATA COMMUNICATION SYSTEM 680

With the 680 series options, the PDP-8 computer becomes an economical device for buffering, formatting, and transmission of data from several Teletypes or other data terminals and large scale computers. One of the most important jobs of a 680 System is simply buffering multiple Teletype lines. Assuming only minor data handling before transmission to the large scale computer, a 680 System can handle up to 128 5-bit lines at 50 baud. (Exact timing is shown in the Timing Table in this bulletin.) Although the 680 System programming described in this bulletin includes only the handling of Teletype lines, programs for packing and unpacking of lines or messages are easily prepared.

The 680 System is designed to concentrate Teletype data to or from multiple Teletype lines, in serial bit format. Programs require two special IOTs plus clock hardware and their associated IOTs which are described in this bulletin. Though the programming assumes Teletypes are being used, there is no reason why other data transmission devices, which present information in the same serial bit format, could not be attached to a 680 System. Subroutines as presently written are designed for the 8-bit Teletype code, the 5-bit Teletype code, or a combination of both. They can also handle mixed speeds on either 8-bit or 5-bit lines with minor changes. Full duplex lines are assumed but the subroutines will work with half duplex lines providing the user handles the expected echo.

SYSTEM DESCRIPTION

The 680 System hardware and software interact to handle up to 128 full duplex lines. Figure 1 is a block diagram of a typical 680 configuration. Fifteen lines are assumed; eight are local lines, and seven are remote.



NOTES
(A) IF PRIVATE LINE IS USED, 791 OR 635A POWER SUPPLY IS AVAILABLE; 687 MONITOR AND 688 TERMINAL PANELS ALSO AVAILABLE FOR PRIVATE LINES.
(B) ADDITIONAL INTERFACE MODULES NEEDED FOR DATAPHONE

Figure 1 680 System Block Diagram

Data Line Interface

The 681 Data Line Interface provides the PDP-8 with the capability of transmitting and receiving data over a serial transmission system using standard Teletype start stop code. To facilitate serial transmission and reception, two special purpose instructions are added to the PDP-8 repetoire:

1. TTI (Teletype In) This is a complex memory reference instruction which deals with two locations in core memory and also with the incoming Teletype line. The flow chart shown in Figure 2 will aid in understanding the operation of this instruction. The two memory locations referred to by this instruction are those immediately following the instruction. They are used to store the Line Status Word (LSW) and the Character Assembly Word (CAW) in the order shown below:

Y	TTI Instruction
Y+1	LSW
Y+2	CAW

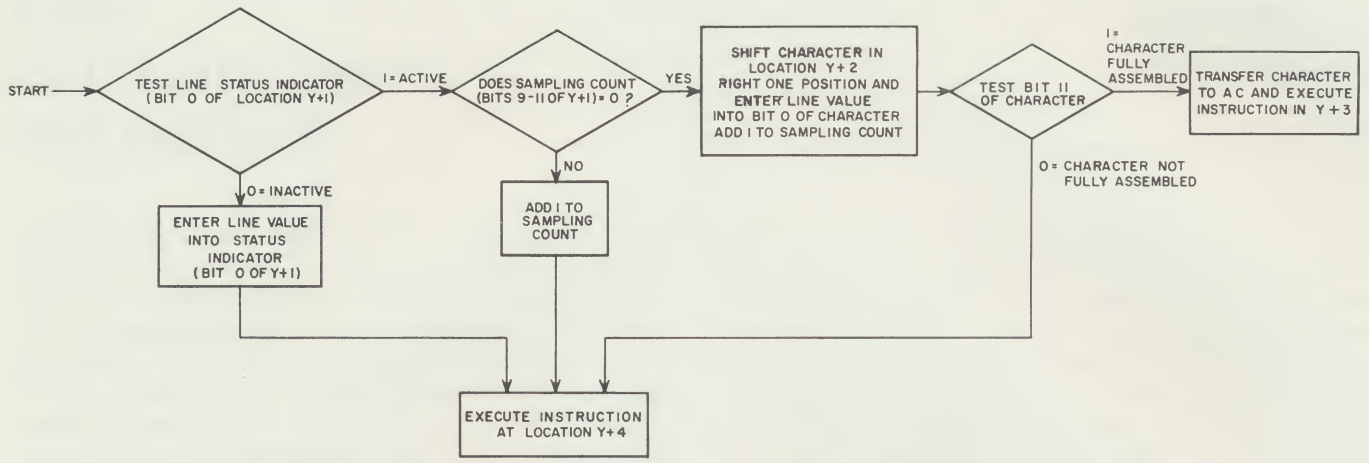


Figure 2 Flow Diagram TTI Instruction

Bits in the line status word are assigned to record the active or inactive state of the line and a real time counter which determines when line sampling should take place. The format of the LSW is shown below:

0 1 2 3 4 5 6 7 8 9 10 11

Active Count

Bits 1-8 of the line status word are not used. The character assembly word is used to store partially assembled characters. Individual bits from the incoming line enter at the left or most significant bit and are shifted to the right during the process of assembly.

The TTI instruction is normally executed following receipt of an interrupt from the real time clock which is set to interrupt the program at a rate equal to eight times the serial bit rate of the incoming line. When executed, the TTI instruction causes the next location in memory to be accessed and examined. This location contains the line status word. The first bit examined is the active bit (bit 0). If it is equal to zero indicating that the line was inactive when last tested, the current contents of the line will be set into the active bit. That is, if a start bit is currently being received, the active indicator will be set to one. If no start bit is being received it will remain a zero. In either event the character assembly word will be skipped over and the next instruction will be executed. (Figure 3, a timing diagram for a typical Teletype line, will aid in understanding the action of the instruction.) Should examination of the active bit indicate that the line is already active, one will be added to the count portion of the LSW and unless the resulting count equals 4 the CAW will be skipped. When the count becomes equal to 4 indicating that 4 clock interrupts have been received since the line first became active or that 4/8 of a bit time has elapsed we know that the center of the bit has been reached and it should be sampled. Thus the character assembly word is accessed, its contents are shifted right one place and the bit presently being received on the line is set into the leftmost position of the CAW. After the first bit has been received it will require 8 clock periods until the count is again equal to 4 and thus each bit in the serial train will be sampled within 12-1/2% of its center.

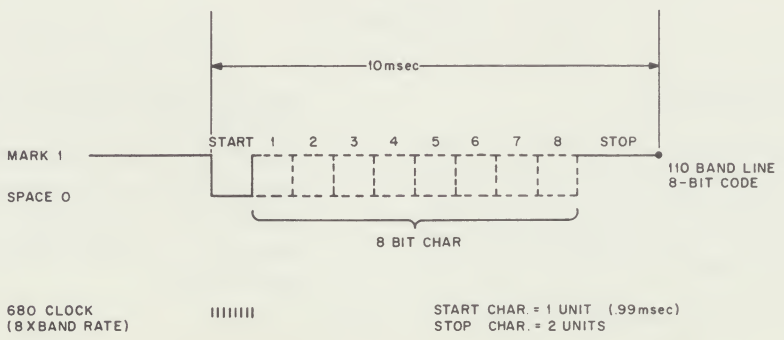


Figure 3 Typical TTY Line Timing

2. TTO (Teletype Out) This instruction acts only on the accumulator and the outgoing line. It is executed during a single memory cycle. Its effects are to shift the contents of the accumulator one position to the right and to transmit the rightmost bit on the outgoing line via the W750. Since a bit is transmitted every time this instruction is executed it should be programmed to occur only after 8 clock interrupts have been received since the last output.

685 SERIAL LINE MULTIPLEXER

The 685 is simply a switch which allows the 681 to be connected to any one of 64 Teletype lines. To select a line, the accumulator is set first to the number of the desired line and its contents are then transferred by an IOT command onto the line selection register of the 685. The line selection register may be loaded at any time with a new address for random scans or incremented by a command which may be microprogrammed with the TTI or TTO instructions. Incrementing is used for high speed sequential scans. This unit also contains a flip-flop for each outgoing line. This flip-flop is set or cleared by a TTO instruction and is used to hold the line in the proper state until the next TTO is executed.

PROGRAMMING

There are three groups of IOTs provided by the hardware:

1. IOTs which handle the characters on a serial bit basis.
2. IOTs which handle the line register.
3. IOTs which handle the clock.

The IOTs and program sequences shown are used in the subroutines only, and are not used anywhere in the main program. They are described for information only.

Character Handling IOTs

1. Teletype Output Command - The Teletype Output Command (TTO, 6404) shifts the contents of the accumulator right one place, sends the previous contents of bit 11 to the Teletype line specified by the line register, and brings a zero into bit 0 of the accumulator. The program sequence to output a word might therefore look as follows:

```
TAD   CHAR    /pick up character to output
TTO           /shift and output one bit
DCA   CHAR    /save remainder of character
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The sequence shown assumes that the line register has been loaded with the correct line number using the line register commands described in Line Register Return.

2. Teletype Input Command - The Teletype Input Command (TTI, 6402) is used to bring the bits coming over the line into memory and assemble the bits into one Teletype character. The TTI command uses three memory locations as follows:

```
TTI
0      /status and counter word
2000   /character assembly word (for 8-bit code)
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The computer returns to TTI + 3.

The character assembly word is preset so that a 1 will appear in bit 11 when the entire character including one stop bit has been shifted in. The subroutines, finding a one in bit 11, assume that an entire character has been read, place the character in its own internal buffer together with the line number it came from, and reinitializes the TTI command by resetting the status word to 0 and the character assembly word to the proper number. The program only checks 1/8th of the lines (1/4 for 5-bit codes) at each clock pulse for completion. Unlike the TTO command the TTI command is executed for all lines at each clock interrupt. However, once the incoming character is started (i.e., bit 0 of the status word = 1) the first bit (the start code) is read at the fourth pulse and each succeeding bit is read at the eighth pulse thereafter, thus guaranteeing that the bit is read at the optimum time.

3. Teletype Increment Command - The Teletype Increment Command (TTINCR, 6401) increments the line register. This is normally used as a microprogrammed version of either the TTI or TTO commands described previously and when used in that manner the incrementing of the line register is done first followed by the normal function of the command issued.

Line Register Command

1. Clear the Line Register - The Clear the Line Register command (TTCL, 6411) sets the line register to all zeros (i.e., to line number 0).

2. Set the Line Register - The Set the Line Register command (TTSL, 6412) sets the line register equal to the low order 7 bits of the accumulator and clears the accumulator.

3. Read the Line Register - The Read the Line Register command (TTRL, 6414) reads the line register into the accumulator. It reads in 7 bits only, and does not clear or destroy any other bits in the accumulator.

Clock IOTs

1. Turn Clock On - The Turn Clock On IOT (TTXON, 6422) turns the appropriate clock on and lowers the clock flag.

2. Turn Clock Off - The Turn Clock Off IOT (TTXOFF, 6424) turns the appropriate clock off and lowers the clock flag.

3. Skip on Clock Flag - The Skip Command (TXSKP, 6421) skips on the appropriate clock flag.

NOTE: In all three mnemonics above, the X would normally be replaced by a number indicating the clock being used in the Teletype subroutines. Additional clock IOTs, if using more than one speed or character size, would use the numbers 643X, 644X, etc.

SUBROUTINE SPECIFICATIONS

The subroutines as presently coded occupy 400 octal locations plus space for internal buffering of the input and output characters and space for the TTI instructions. In addition, space is used in memory page 0 and a limited number of auto-index registers are used as explained below. Within the limits described the program or programs can be placed anywhere in the PDP-8 memory. The total amount of memory used including the auto-index registers and the locations in page 0 is as follows:

$$422_8 + 7N \text{ (for 8-bit)} \quad \text{or}$$
$$434_8 + 7N \text{ (for 5-bit)}$$

where N is the amount of lines specified to the subroutines. In the descriptions of the individual pseudo-commands or registers which follow, the assumption is made that the 8-bit set of subroutines are being used. If the 5-bit subroutines are being used all of the tags mentioned should substitute a 5 for the 8 shown. If both an 8-bit and 5-bit system are being used, both sets of subroutines are necessary and all tags and requirements must be duplicated for the second system. At present, coding is available for a single 8-bit system and for 2 different 5-bit systems to allow the programmer to assemble all of the necessary components with his own main program at one time. Assumptions are made about the clock IOTs which may require changing for actual applications.

For further information, refer to DEC-35-S-A and DEC-35-S-B in DEC Program Library.

TIMING

The table below indicates the percentages of machine time used for various types of systems and is as accurate as presently possible. Any additional features which may be required for the Teletype handling would add appreciably to the times shown. For the user's convenience, the formulas used for calculating the times are included so that times for systems with an intermediate number of lines or with combinations of lines can be easily calculated. For combined systems, simply add up the percentages used for each component.

TIMING TABLE

Numbers indicate the percentage of available machine time used in the average case.

No. of Lines	8-Bit 110 Baud*	5-Bit 50 Baud**	5-Bit 75 Baud***
32	34.1%	20.0%	30.0%
64	57.7%	35.1%	52.7%
96	81.3%	50.3%	75.5%
128	104.9%	65.5%	98.3%

* Formula Used: Where N = the number of lines, the 8-bit subroutines require an average time of 8.38N + 119.5 μsec.

** Formula Used: Where N = the number of lines, the 5-bit subroutines require an average time of 11.85N + 120 μsec. Clock flags (at 50 baud) occur every 2500 μsec.

***Formula Used: The percentages for 75 baud are merely 1.5 X 50 baud rate. Clock flags occur every 1667 μsec.

APPENDIX 1

LIST OF ITEMS NECESSARY IN THE MAIN PROGRAM

8-Bit	5-Bit	5-Bit (2nd Speed)	Meaning
TT8BGN	TT5BGN	TT4BGN	Beginning of subroutine
T8AX1	T5AX1	T4AX1	Auto-index register
T8AX2	T5AX2	T4AX2	Auto-index register
T8AX3			
T8AX3	T5AX3	T4AX3	Auto-index register
	T5AX4	T4AX4	Auto-index register (5-bit only)
TT8PG0	TT5PG0	TT4PG0	Start of area in page 0
T8OBF2	T5OBF2	T4OBF2	Start of 2nd output buffer (length = N)
T81BF	T51BF	T51BF	Start of input buffer (length = 2N)
T81N	T51N	T51N	Start of TTI area (length = 3N + 1)
TTCHAR	TTCHAR	TTCHAR	Character area (appears only once)

APPENDIX 2

680 SYSTEM PRICING

Type	Description	Price
681	Data Line Interface Adds I/O instructions to PDP-8 processor, packaged with C.P. frame, and provides basic interface to PDP-8.	$1,500
682	TTY Connector Panel Optional panels with FLIP CHIP connectors to mate with 64 Teletype FLIP CHIP connectors (2 FLIP CHIP panels). 32 connector version may be ordered for $800.	$1,200
683	Telegraph Level Converter Optional panels for driving long lines. Two panels (FLIP CHIP) accommodate up to 32 full duplex lines. (Does not include G852 dual telegraph level converters.) (2 FLIP CHIP panels.)	$1,200
G852	Dual Telegraph Level Converter Interfaces long telegraph lines to DEC logic levels. Can operate both Neutral and Polar. Two full duplex lines per module.	$ 215
684	Matricon Patchboard For patching 32 full duplex processor lines to 32 full duplex telegraph lines or Teletype lines.	$4,950 each
685	Serial Line Multiplexer Can interface up to 64 full duplex Teletype lines. Accepts Teletype line units. Does not include line units; does include one clock. Three additional clocks may be added. (2 FLIP CHIP panels.)	$4,300
W750	Teletype Line Unit Activates Serial Line Multiplexer (685). One unit required per line.	$ 100
686	Line Sampling Clock Unit Additional clock for 685 multiplexer; for intermixing speeds, 3 may be added.	$ 450
791	Power Supply (Polar or Neutral ±80v) Line Power Supply.	$ 400
635A	Power Supply (120v Neutral) Line Power.	$ 500

687	Line Monitor Panel Switch and meter panel which measures outgoing telegraph line currents of the G852. Used in conjunction with 688.	$ 450
688	Line Terminator Panel Contains four telegraph connector terminals and 64 variable resistors for 32 duplex lines.	$1,635

NOTE: Add cabinet as required for 680 housing.

APPENDIX 3

PRICING EXAMPLE

680 System with 8 local plus 7 remote lines:

Items	Type	Cost	FC Mounting Panels
1	681 D.L.I.	$1,500	-
1	685 S.L.M.	4,300	2
15	W750 T.L.U. @ $100 each	1,500	-
1	683 TLC	1,200	2
4	G852 D.T.L.C. @ 215	860	-
		$9,360	4

BASIC SYSTEM

1. In addition, 684 Patchboard, and 682 Connector Panels may be added.

2. 791 and 635A Power Supplies, plus 687 Monitor and 688 Terminator Panels are available for use with private lines.

3. Add cost of interface to dataphone as necessary.